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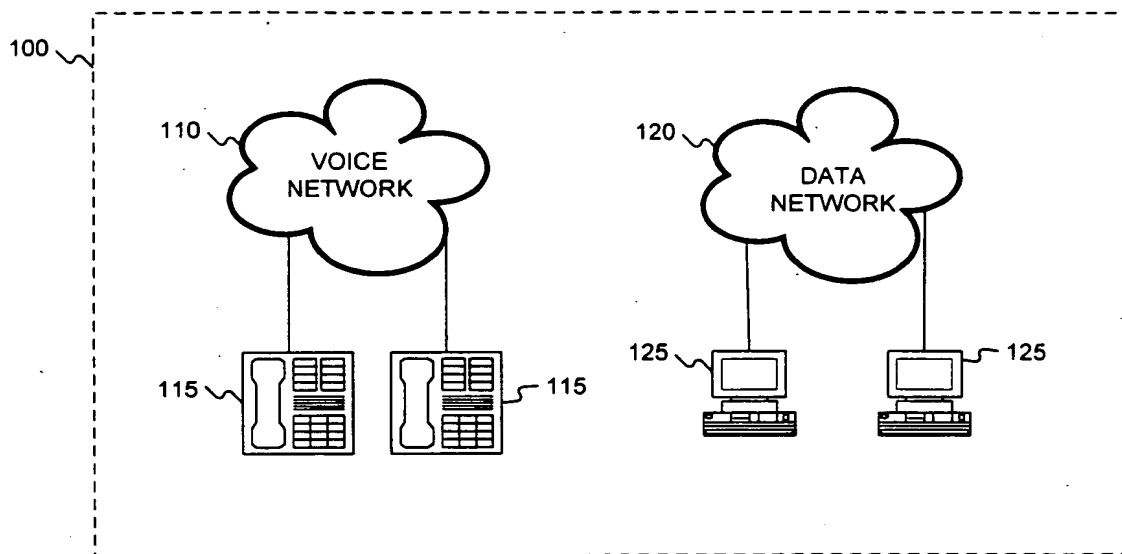
[illegible]

FIG. 1
PRIOR ART

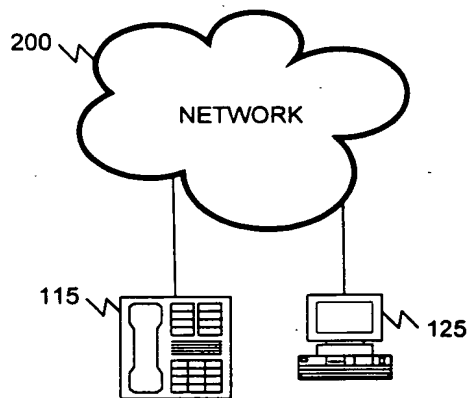


FIG. 2

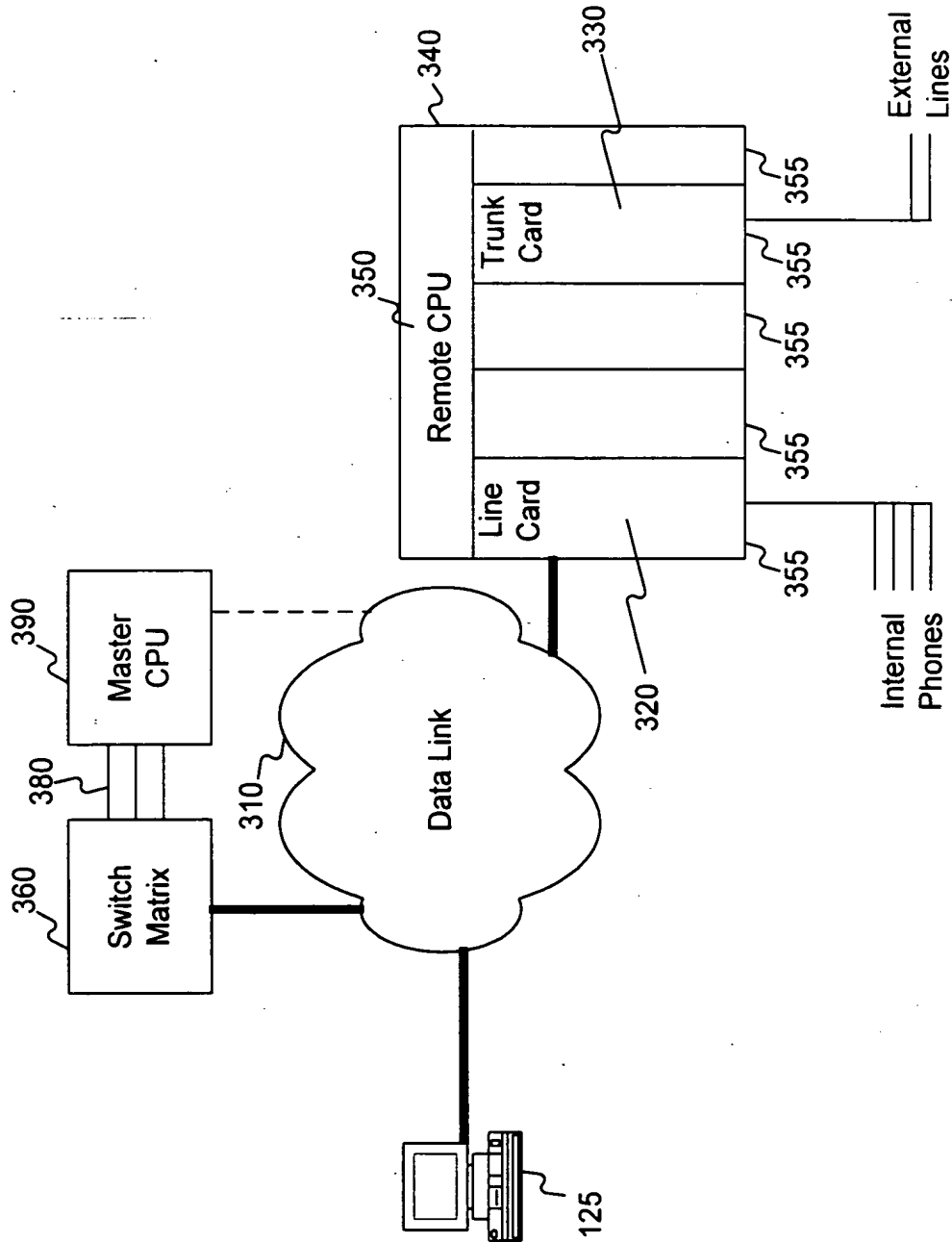


FIG. 3

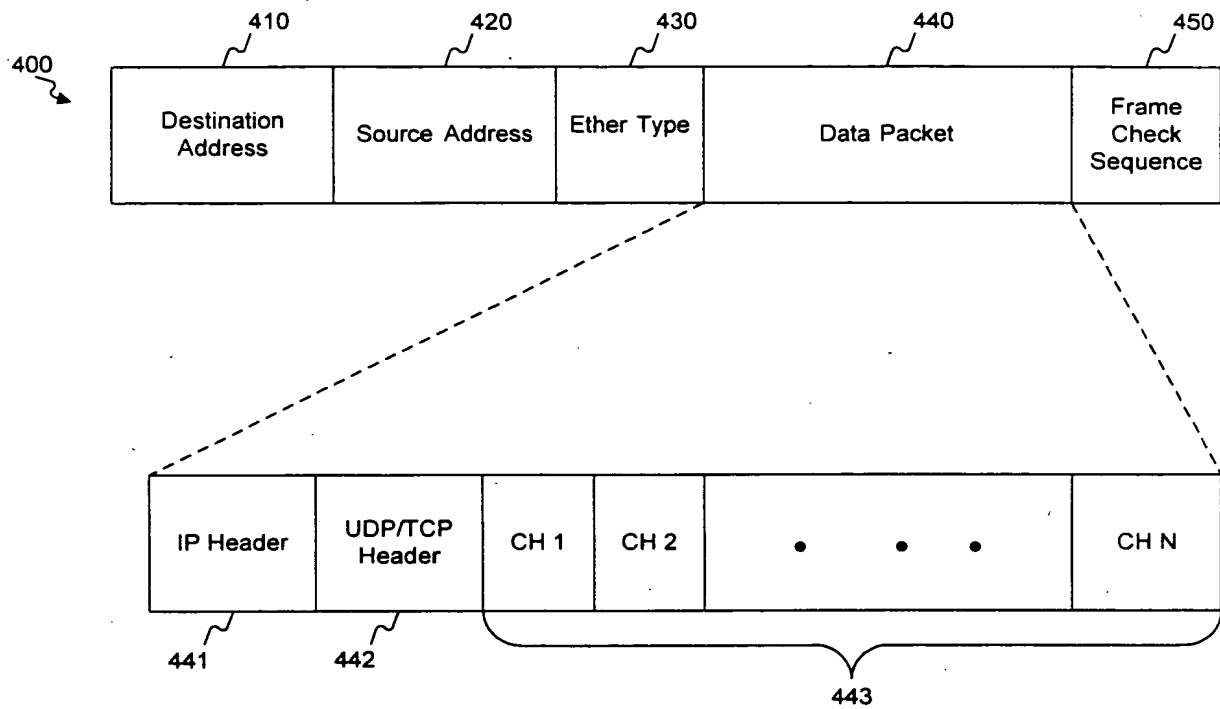


FIG. 4

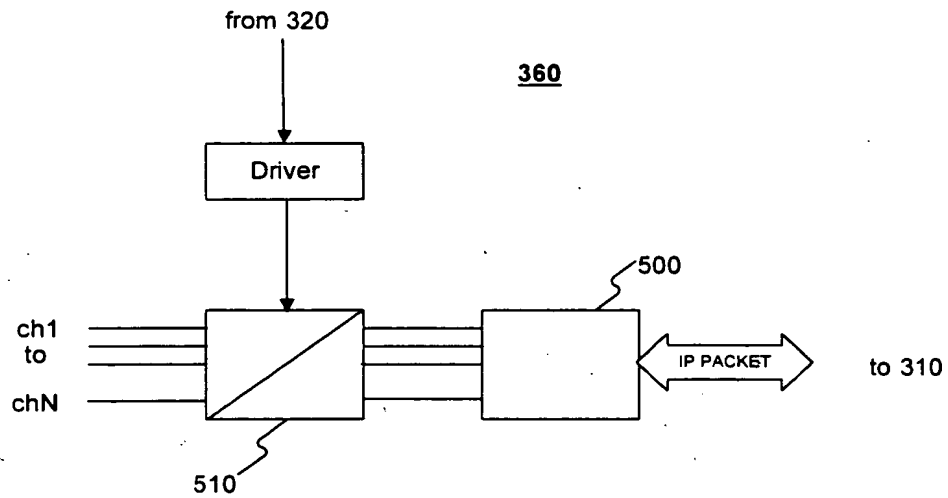


FIG. 5

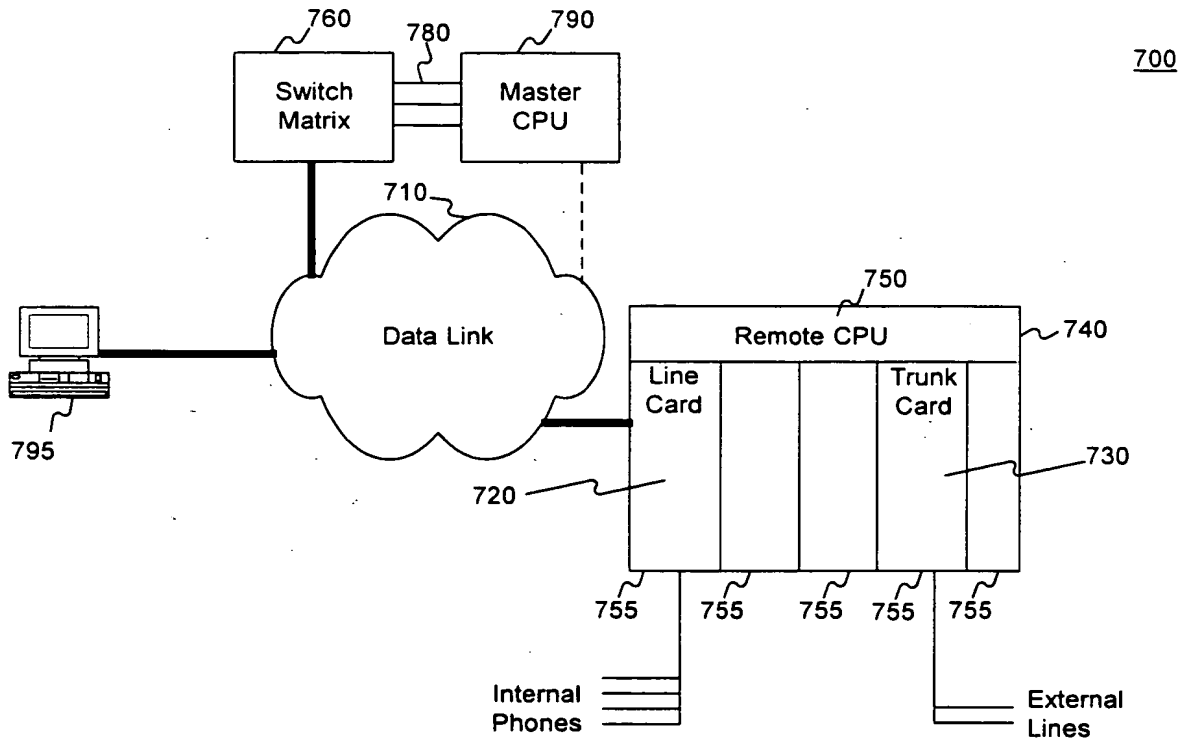


FIG. 6

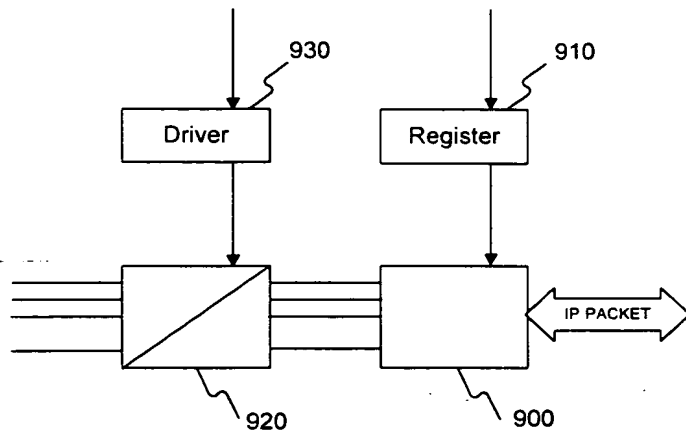


FIG. 8

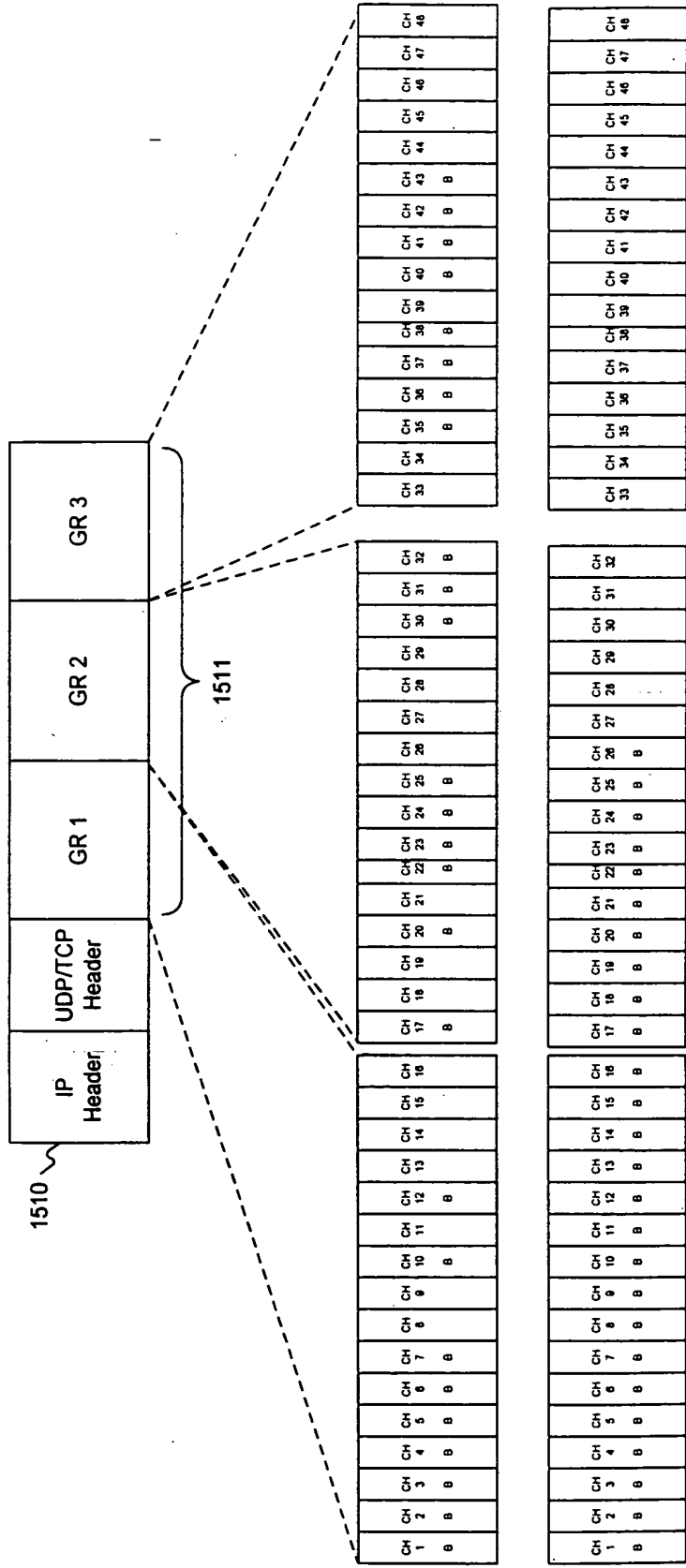


FIG. 12

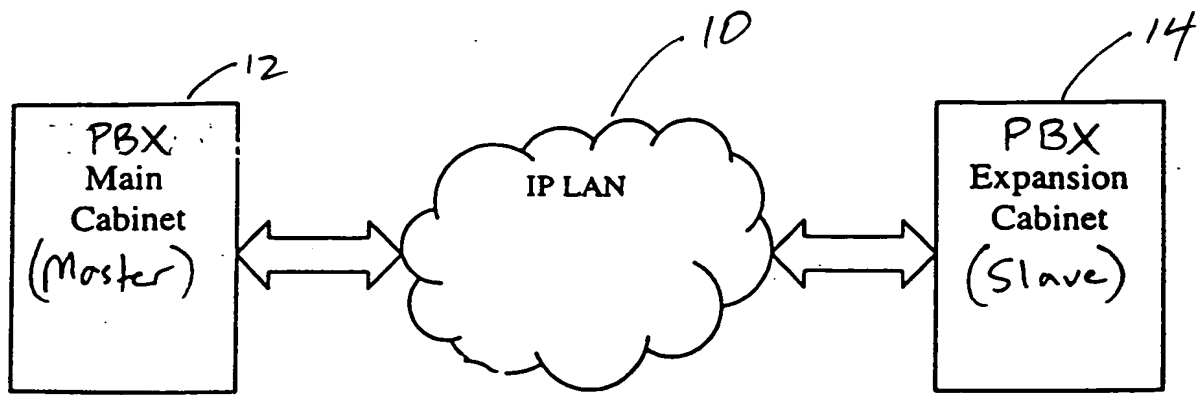


FIG. 13

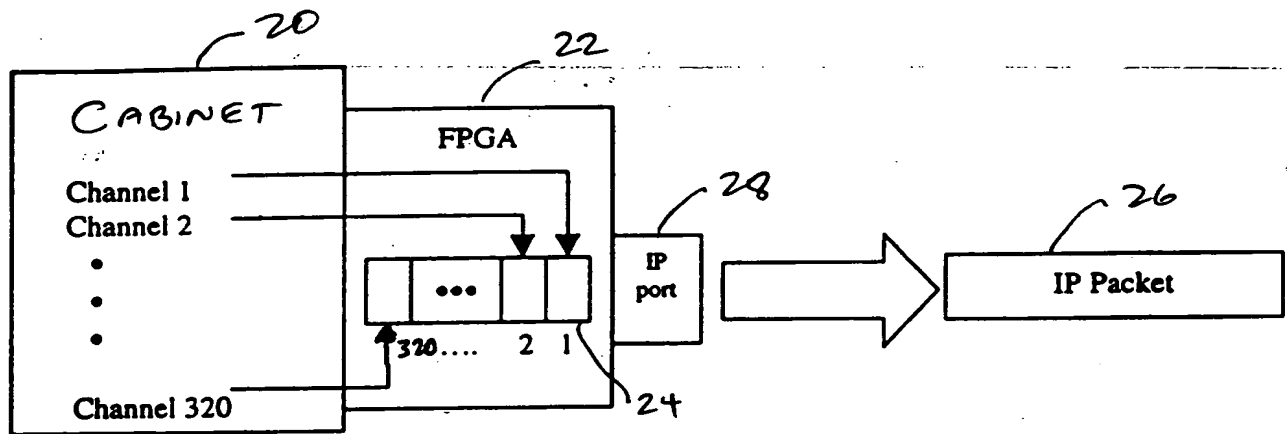


FIG. 14

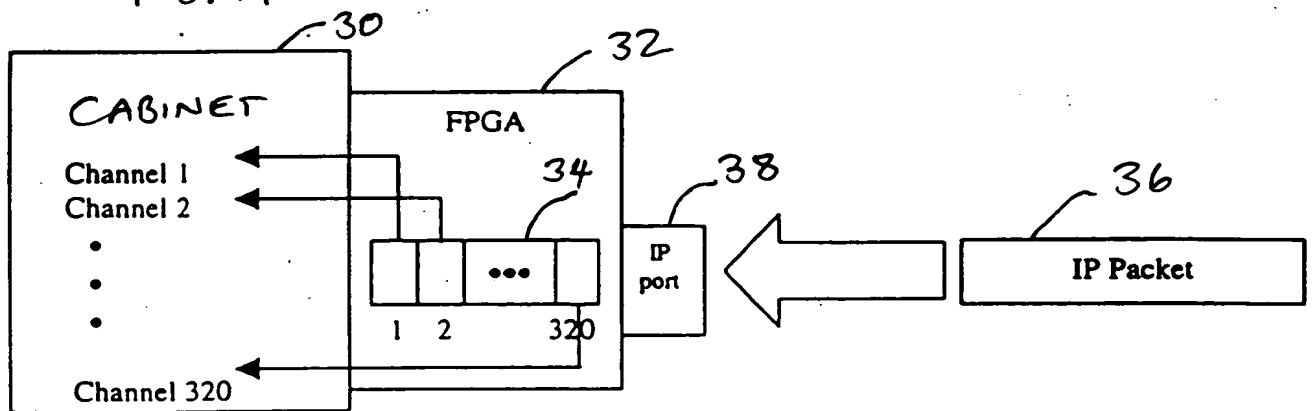


FIG. 15

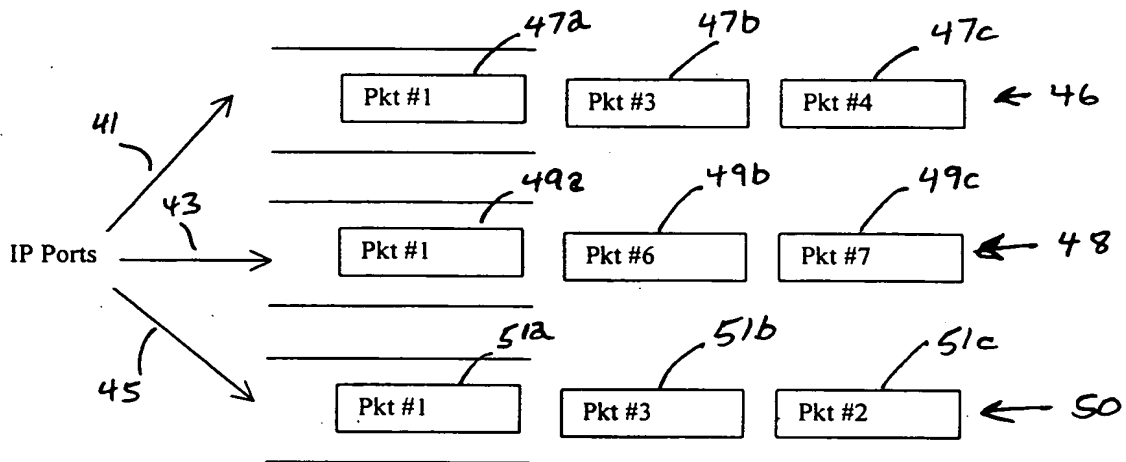


FIG. 16a

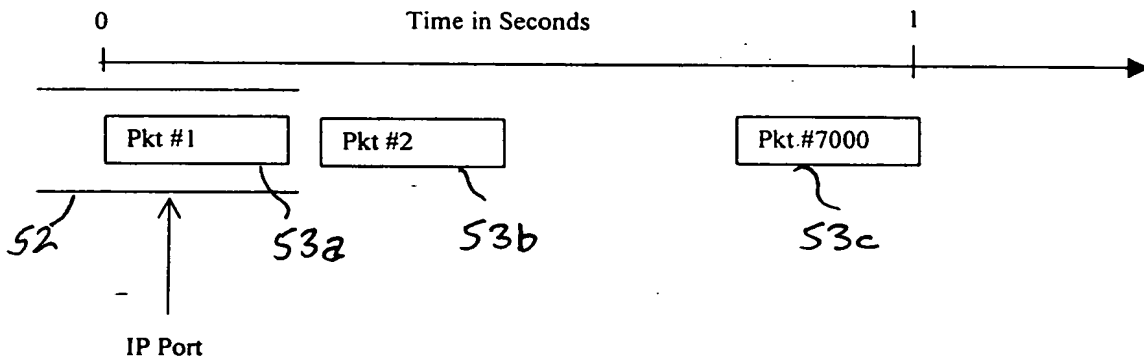


FIG. 16b

2025 RELEASE UNDER E.O. 14176

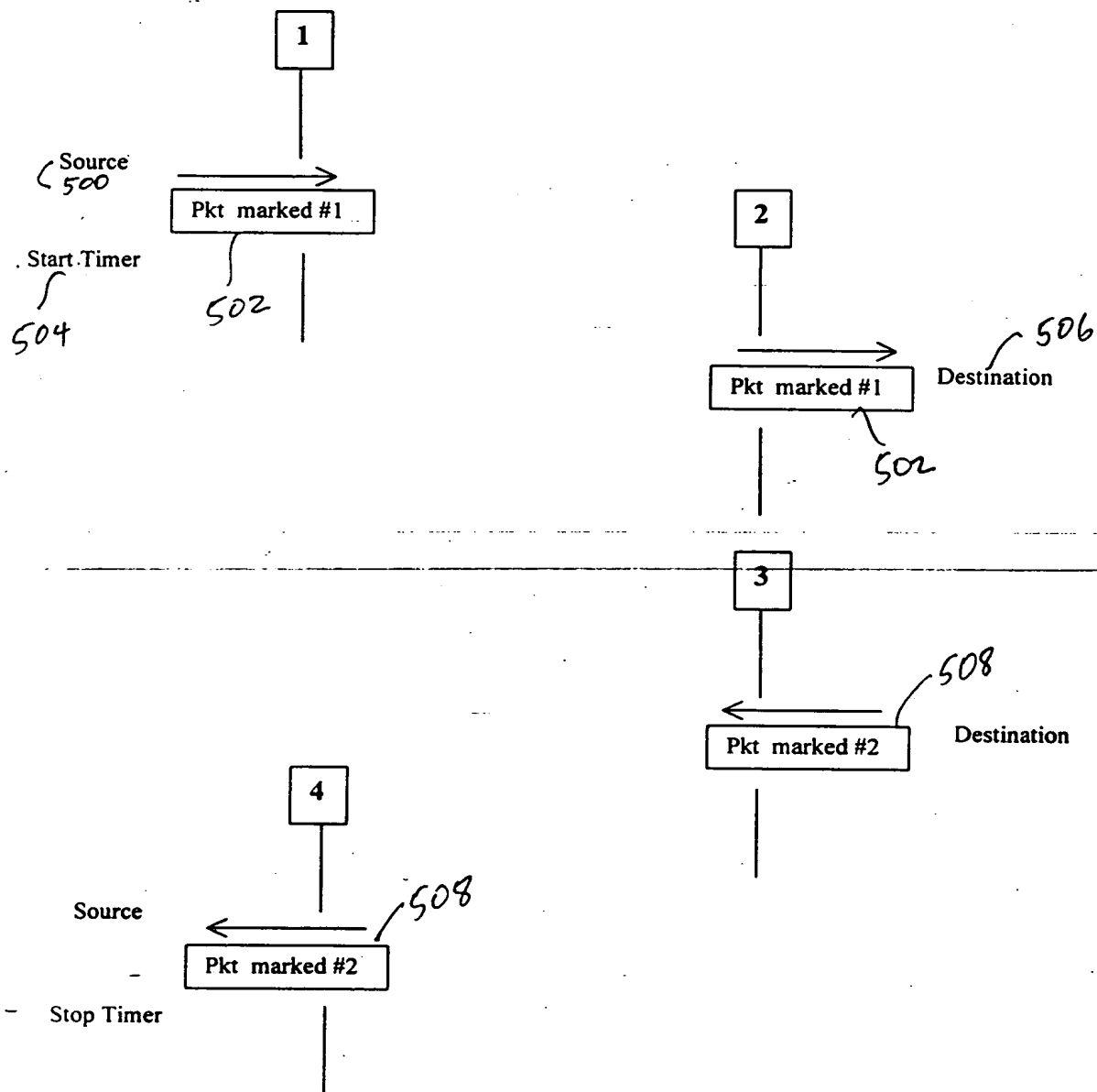


FIG. 17

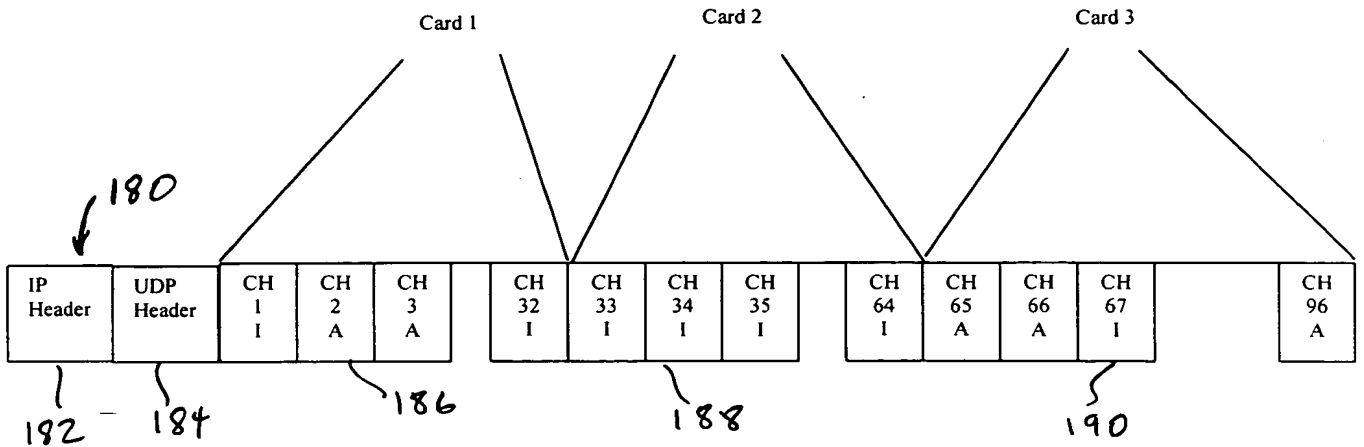


FIG. 182

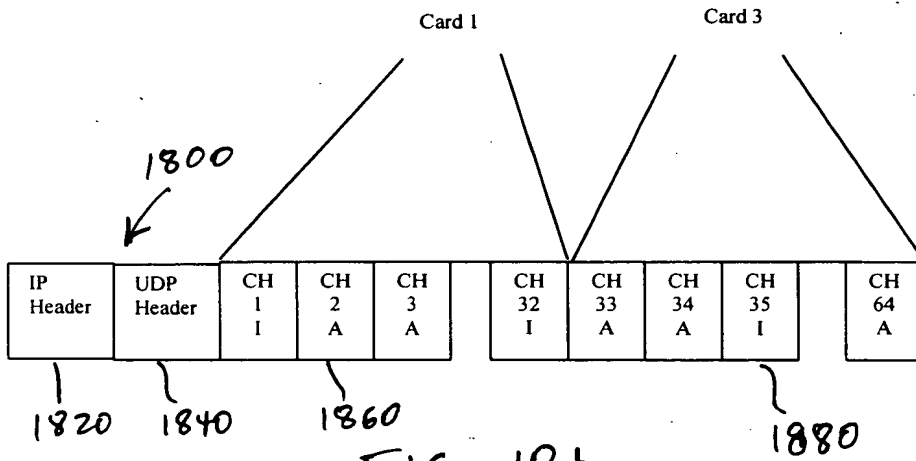
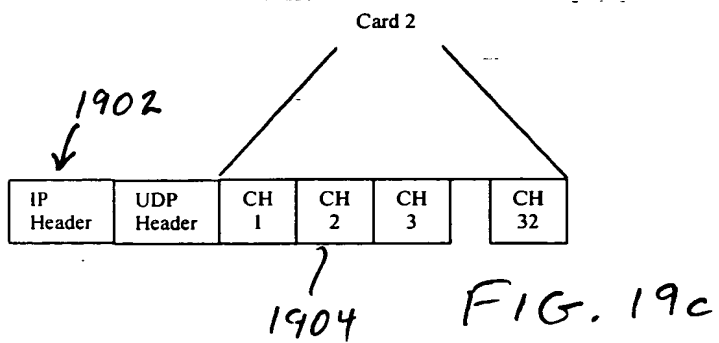
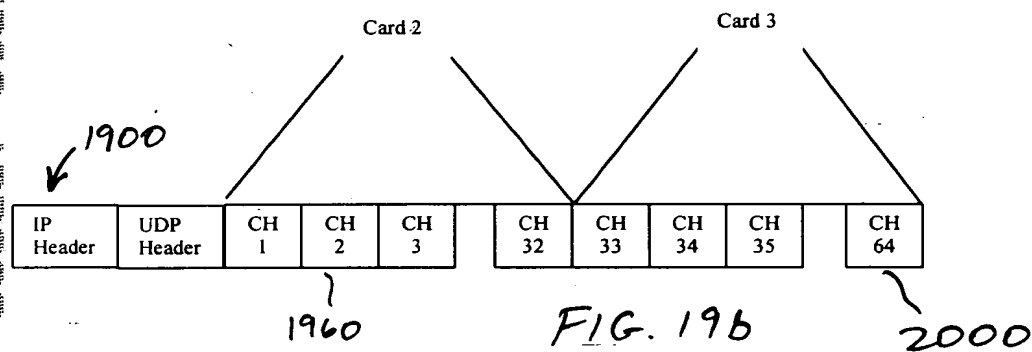
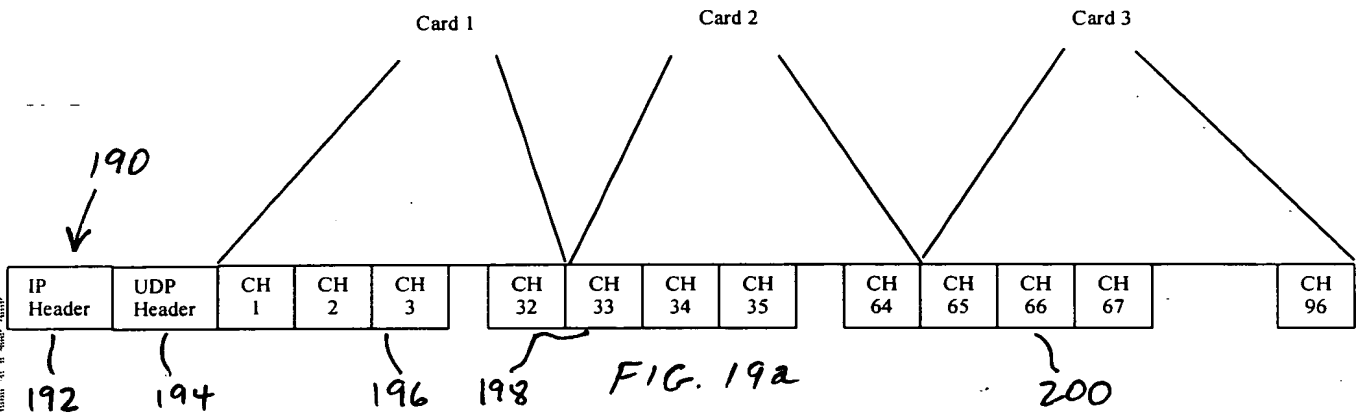


FIG. 18b

6061 6352152



```

graph TD
    60[Wait for complete interval] --> 62[Read PLC]
    62 --> 64{ (PLC > Thr1) & (ΔPLC > 0) }
    64 -- Yes --> 66[Increment PLC_Flag]
    64 -- No --> 72[Reset PLC_Flag]
    66 --> 68{ PLC_Flag > thr2 }
    68 -- Yes --> 70[Enable Bandwidth Optimization]
    70 --> 72
    72 --> 60

```

FIG. 20

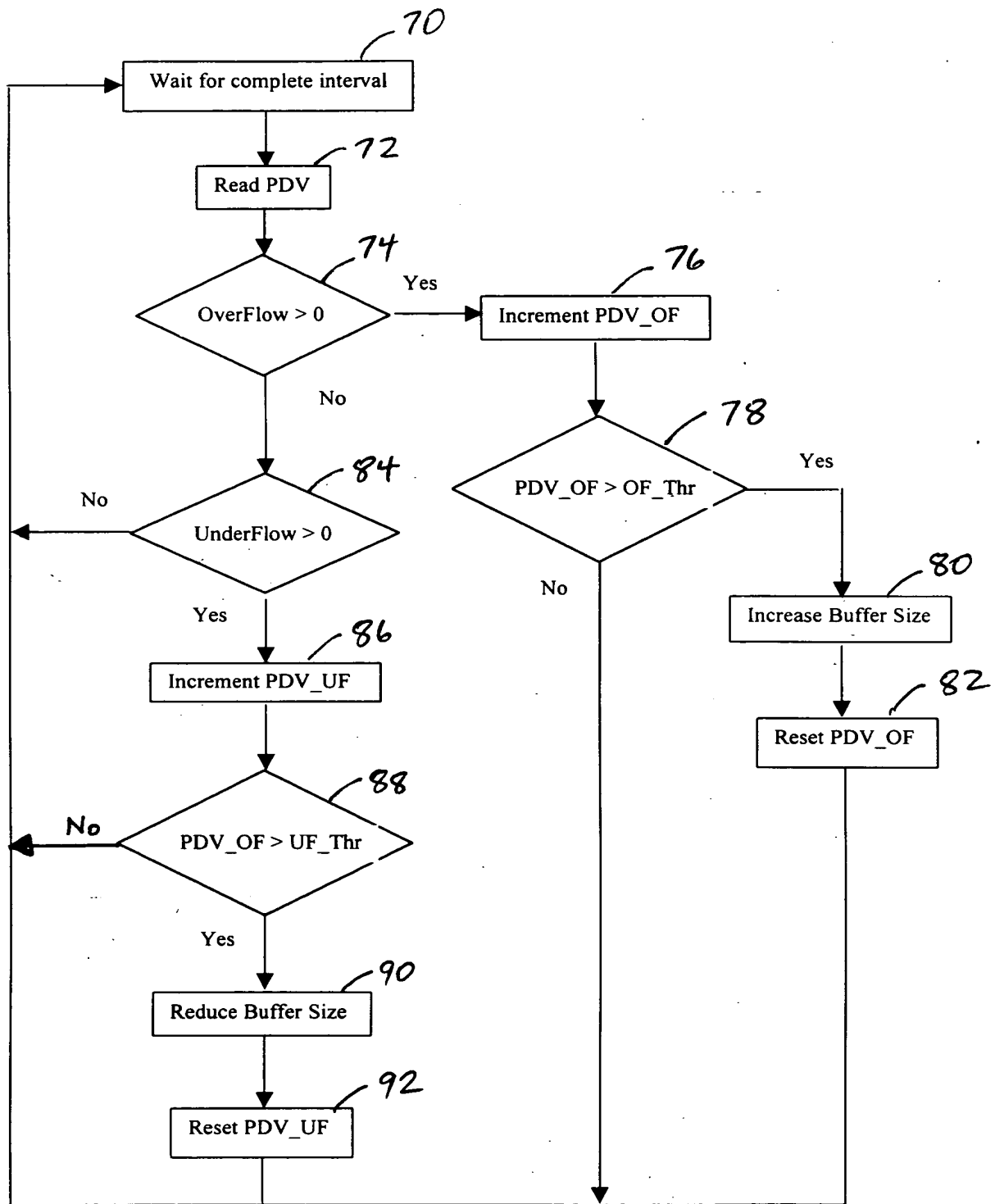


FIG. 21

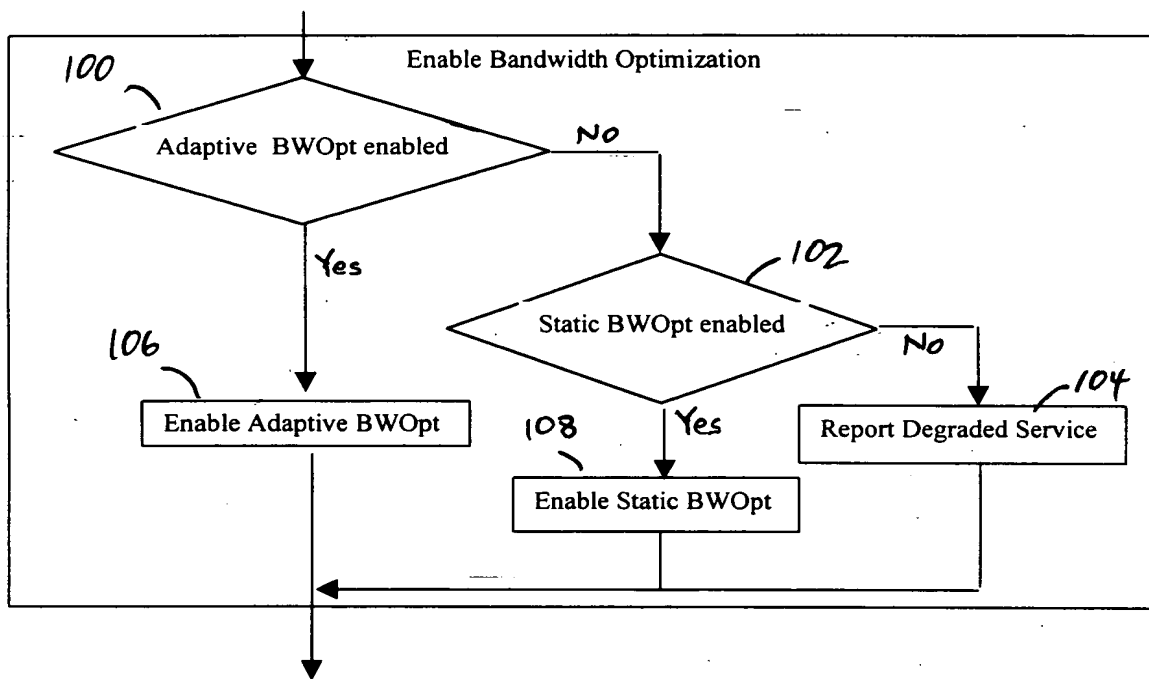


FIG. 22